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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,407	10/01/2003	Robert C. Chang	SANDP043	8052

67674 7590 02/06/2008

ANDERSON, LEVINE & LINTEL fbo SANDISK CORPORATION
14785 PRESTON ROAD
SUITE 650
DALLAS, TX 75254

EXAMINER	
LAMARRE, GUY J	
ART UNIT	**PAPER NUMBER**
2112	

MAIL DATE	DELIVERY MODE
02/06/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	10/676,407	CHANG ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/3/08*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Pursuant to 35 USC 131, **Claims 1-38** are presented for examination.

Response to Arguments

2. Applicants' arguments have been fully considered, and are deemed persuasive. As result, the restriction requirement is removed.

Claim Rejections - 35 USC § 103

3. **Claims 1-38** are rejected under 35 U.S.C. 103(3) as being obvious over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) and **Klayman et al.** (USPN 5699365).

As per Claims 1-38, Admitted Prior Art substantially teaches the claimed error correction for memory system on page 1 line 20 – page 3 last line, said memory comprising a redundant area of a page associated with a physical block of a non-volatile memory, said redundant area comprising byte including error correction code (ECC) information.

Not specifically described in detail in **Admitted Prior Art ,** is the approach whereby the ECC is made dynamically alterable based on plural criteria including noise/read/write/erase threshold levels.

However, Klayman et al., in an analogous art, teaches an adaptive error correction approach for data communication/transfer in a multimedia environment at col. 1 line 12 wherein such dynamic ECC schemes are applied, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45, e.g., '*the method illustrated in FIG. 4 may be programmed and stored, as a set of program instructions for subsequent execution, in the primary station 101 and, more particularly, in each of the processors 130 (with their associated memories 131), utilizing packet or bit error data from the forward error correction decoding performed by the corresponding receivers 135. To the extent that adjustable and dynamic forward error correction capability is necessary or desirable in the downstream direction, the*

method illustrated in FIG. 4 also may be programmed and stored, also as a set of program instructions for subsequent execution, in the processor 150 and memory 155 of a secondary station 110, such as secondary station 110.sub.n illustrated in FIG. 3.'

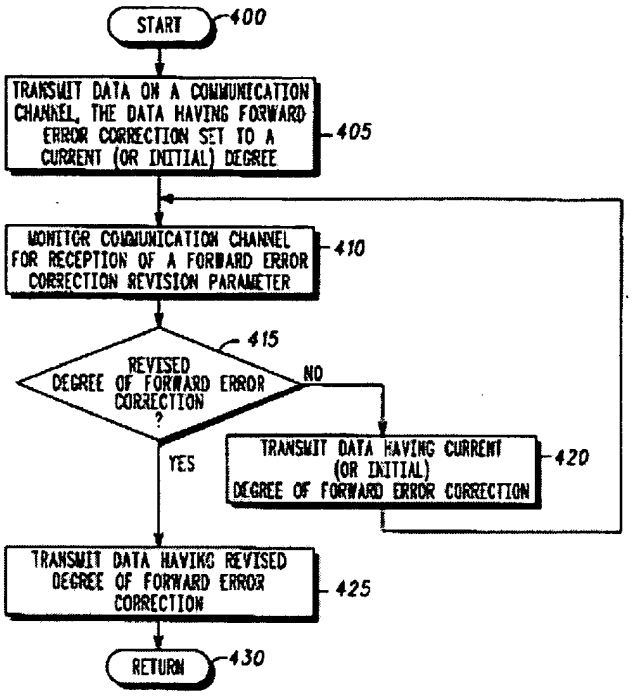

FIG. 5

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Admitted Prior Art** by including therein dynamic ECC *metrics* as taught by **Klayman et al.,** because such modification would provide the procedure disclosed in **Admitted Prior Art** with a technique whereby data transfer is optimized via the dynamic adaptive forward error correction. See **Klayman et al.**, Fig. 5:Bloch 425.

As per Claim 1, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37, col. 7 lines 9 and 63 – threshold-, col. 9 line 10, col. 12 line 45-- the claimed method for dynamically configuring a

redundant area of a page associated with a physical block of a non-volatile memory of a memory system, the method comprising: determining whether at least one byte associated with the redundant area is to be altered, the at least one byte including error correction code (ECC) information associated with a first ECC algorithm; and altering the at least one byte responsive to determining that the at least one byte is to be altered, wherein altering the at least one byte includes altering the at least one byte to include ECC information associated with a second ECC algorithm.

As per Claim 2 , **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37, col. 7 lines 9 and 63 – threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 1 wherein the first ECC algorithm is a 1-bit ECC algorithm.

As per Claim 3, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37, col. 7 lines 9 and 63 – threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 2, wherein the at least one byte includes ECC information associated with the first ECC algorithm—and includes: approximately three bytes arranged to be used to correct an error associated with a first group of bytes of a data area of the page, approximately three bytes arranged to be used to correct an error associated with a second group of bytes of the data area, and approximately two bytes arranged to be used to correct an error associated with the redundant area.

As per Claim 4, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63

–threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 2 wherein the second ECC algorithm is a 2-symbol ECC algorithm.

As per Claim 5 , **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 4 wherein ~ the at least one byte includes ECC information associated with the second ECC algorithm and includes: approximately five bytes arranged to be used to correct at least one error associated with the data area of the page, and approximately three bytes arranged to be used to correct at least one error associated with the redundant area.

As per Claim 6 , **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 1 further including: obtaining at least one bit which is arranged to indicate a number of times the physical block has been erased from the redundant area, wherein determining whether the at least one byte is to be altered includes determining whether the at least one bit is approximately equal to a predetermined value.

As per Claim 7 , **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 1 wherein the at least one bit includes information associated with an erase count of the physical block.

As per Claim 8 , **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 1 wherein the at least one byte associated with the redundant area is to be altered includes determining whether a number of erase cycles undergone by the physical block has reached a threshold level.

As per Claim 9 , **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 1 wherein altering the at least one byte includes storing the at least one byte which includes ECC information associated with the second ECC algorithm in the redundant area.

As per Claim 10, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 1 wherein the non-volatile memory system is one of an embedded system, a Smart Media card, a Compact Flash card, a Secure Digital Card, and a MultiMedia card.

As per Claim 11, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system comprising: a non-volatile memory, the non-volatile memory including a physical block, wherein the physical block has a page with a data area and a redundant area;

code devices that cause a determination to be made as to whether at least one byte associated with the redundant area is to be altered, the at least one byte including error correction code (ECC) information associated with a first ECC algorithm;

code devices that cause the at least one byte to be altered responsive to determining that the at least one byte is to be altered, wherein the code devices that cause the at least one byte to be altered include code devices that cause the at least one byte to be altered include ECC information associated with a second ECC algorithm; and

a memory section that stores the code devices.

As per Claim 12, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 11 wherein the first ECC algorithm is a 1-bit ECC algorithm.

As per Claim 13, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 12 wherein the at least one byte includes ECC information associated with the first ECC algorithm, and includes: approximately three bytes arranged to be used to correct an error associated with a first group of bytes of a data area of the page, approximately three bytes arranged to be used to correct an error associated with a second group of bytes of the data area, and approximately two bytes arranged

to be used to correct an error associated with the redundant area.

As per Claim 14, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 12 wherein the second ECC algorithm is a 2- symbol ECC algorithm.

As per Claim 15, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 14 wherein ~ the at least one byte includes ECC information associated with the second ECC algorithm, and includes: approximately five bytes arranged to be used to correct at least one error associated with the data area of the page, and approximately three bytes arranged to be used to correct at least one error associated with the redundant area.

As per Claim 16, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 11 further including: code devices that cause at least one bit arranged to indicate a number of times the physical block has been erased to be obtained from the redundant area, wherein the code devices that cause a determination to be made as to ~ whether the at least one byte is to be altered include code devices that cause a determination to be made as to whether the at least one bit is approximately equal to a predetermined value.

As per Claim 17, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 11 wherein the at least one bit includes information associated with an erase count of the physical block.

As per Claim 18, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 11 wherein the code devices that cause a determination to be made as to Mae--n whether the at least one byte associated with the redundant area is to be altered currently amended code devices that cause a determination to be made as to whether a number of erase cycles undergone by the physical block has reached a threshold level.

As per Claim 19, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 11 wherein the code devices that cause the at least one byte to be altered include code devices that cause the at last one byte which includes ECC information associated with the second ECC algorithm to be stored in the redundant area.

As per Claim 20, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 11 wherein the

non-volatile memory system is one of an embedded system, a Smart Media card, a Compact Flash card, a Secure Digital Card, and a MultiMedia card.

As per Claim 21, Admitted Prior Art discloses, at page 1 line 20 – page 3 last line, -Also See Klayman et al., e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system comprising: a non-volatile memory, the non-volatile memory including a physical block, wherein the physical block has a page with a data area and a redundant area; means for determining whether at least one byte associated with the redundant area is to be altered, the at least one byte including error correction code (ECC) information associated with a first ECC algorithm; means for altering the at least one byte responsive to determining that the at least one byte is to be altered, wherein altering the at least one byte includes altering the at least one byte to include ECC information associated with a second ECC algorithm.

As per Claim 22, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 21 wherein the first ECC algorithm is a 1-bit ECC algorithm and wherein the at least one byte includes ECC information associated with the first ECC algorithm, and include approximately three bytes arranged to be used to correct an error associated with a first group of bytes of a data area of the page, approximately three bytes arranged to be used to correct an error associated with a second group of bytes of the data area, and approximately two bytes arranged to be used to correct an error associated with the redundant area.

As per Claim 23, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 22 wherein the second ECC algorithm is a 2-symbol ECC algorithm, and wherein ~ the at least one byte includes ECC information associated with the second ECC algorithm, and includes: approximately five bytes arranged to be used to correct at least one error associated with the data area of the page, and approximately three bytes arranged to be used to correct at least one error associated with the redundant area.

As per Claim 24, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 21 further including: means for obtaining at least one bit which is arranged to indicate a number of times the physical block has been erased from the redundant area, wherein the means for determining whether the at least one byte is to be altered include means for determining whether the at least one bit is approximately equal to a predetermined value.

As per Claim 25, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 21 wherein the at least one bit includes information associated with an erase count of the physical block.

As per Claim 26, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63

–threshold-, col. 9 line 10, col. 12 line 45- the claimed memory system of claim 21 wherein the non-volatile memory system is one of an embedded system, a Smart Media card, a Compact Flash card, a Secure Digital Card, and a MultiMedia card.

As per Claim 27, Admitted Prior Art discloses, at page 1 line 20 – page 3 last line, -Also See Klayman et al., e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 – threshold-, col. 9 line 10, col. 12 line 45- the claimed method for processing a page associated with a physical block of a non-volatile memory of a memory system, the method comprising: determining whether at least one byte associated with a first error correction code (ECC) algorithm is to be altered to be associated with a second ECC algorithm, the at least one byte being stored in a redundant area associated with the page; and dynamically configuring the redundant area responsive to determining that the at least one byte is to be altered such that the at least one byte is altered to be associated with the second ECC algorithm.

As per Claim 28, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 27 wherein the first ECC algorithm is a 1-bit ECC algorithm and the second ECC algorithm is a 2-symbol ECC algorithm.

As per Claim 29, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 28 wherein the at least one byte associated with the first ECC algorithm includes approximately three bytes arranged to be used to correct an error associated with a first group of bytes of a data area of the page, approximately three bytes arranged to be used to correct an error

associated with a second group of bytes of the data area, and approximately two bytes arranged to be used to correct an error associated with the redundant area.

As per Claim 30, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 28 wherein the at least one byte is altered to be associated with the second ECC algorithm, and includes approximately five bytes arranged to be used to correct at least one error associated with the data area of the page, and approximately three bytes arranged to be used to correct at least one error associated with the redundant area.

As per Claim 31, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 27 wherein determining whether the at least one byte is to be altered includes determining whether an indicator stored in the redundant area indicates that the at least one byte is to be altered.

As per Claim 32, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 31 wherein the indicator is arranged to indicate a number of times the physical block has been erased, and wherein whether the indicator is approximately equal to a predetermined value, the indicator indicates that the at least one byte is to be altered.

As per Claim 33, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See Klayman et al., e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –

threshold-, col. 9 line 10, col. 12 line 45- the claimed method for dynamically configuring a redundant area of a page associated with a physical block of a non-volatile memory of a memory system, the method comprising: determining whether a set of bits in the redundant area is to be altered, the bits including error correction code (ECC) information associated with a first ECC algorithm, wherein the set of bits are substantially grouped in a first configuration; and altering the set of bits determined responsive to determining that the set of bits is to be altered, wherein altering the set of bits includes altering the set of bits to include ECC information associated with a second ECC algorithm and grouping the set of bits in a second configuration.

As per Claim 34, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 33 wherein the set of bits includes approximately eight bytes and the first configuration includes a first subset of approximately three bytes, a second subset of approximately three bytes, and a third subset of approximately two bytes.

As per Claim 35, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 34 wherein the second configuration includes a first grouping of approximately five bytes and a second grouping of approximately three bytes.

As per Claim 36, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 33 wherein the first

ECC algorithm is a 1-bit ECC algorithm and the second ECC algorithm is a 2-symbol ECC algorithm.

As per Claim 37, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 33 wherein determining whether the set of bits is to be altered includes determining ~ whether an indicator stored in the redundant area indicates that the set of bits is to be altered.

As per Claim 38, **Admitted Prior Art** discloses, at page 1 line 20 – page 3 last line, -Also See **Klayman et al.**, e.g., Figs. 4-5 and col. 4, line 31, col. 5 line 37-RS code-, col. 7 lines 9 and 63 –threshold-, col. 9 line 10, col. 12 line 45- the claimed method of claim 37 wherein the indicator is arranged to indicate a number of times the physical block has been erased, and the indicator indicates that the set of bits is to be altered by having a value approximately equal to a predetermined value.

CONCLUSION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Guy J. Lamarre, P.E
Primary Examiner